Electronic Version
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Claims

[c1] 7. A method for fabricating a memory device, comprising:
forming a buried bit line in a substrate;
forming a gate oxide layer on the substrate;
forming a word line having a capping layer thereon on the gate oxide layer;
forming a spacer on sidewalls of the word line and the capping layer;
forming a dielectric layer on the substrate covering the capping layer;
forming a trench in the dielectric layer located over the buried bit line and exposing a portion of the capping layer;
forming a self-aligned contact opening in the dielectric layer under the trench to expose a portion of the buried bit line, wherein the self-aligned contact opening and the trench together serve as a dual damascene opening; and
filling a conductive material into the dual damascene opening.

[c2] 8. The method of claim 7, wherein an etching rate of the

capping layer is lower than an etching rate of the dielectric layer.

[c3] 9. The method of claim 7, wherein an etching rate of the spacer is lower than an etching rate of the dielectric layer.

[c4] 10. The method of claim 7, wherein the capping layer comprises silicon nitride or silicon oxynitride.

[c5] 11. The method of claim 7, wherein the spacer comprises silicon nitride or silicon oxynitride.

[c6] 12. The method of claim 7, wherein the dielectric layer comprises silicon oxide.

[c7] 13. The method of claim 7, wherein filling the conductive material into the dual damascene opening comprises:
forming a layer of the conductive material covering the dielectric layer; and
removing the conductive material outside the dual damascene opening.

[c8] 14. The method of claim 13, wherein removing the conductive material outside the dual damascene opening comprises performing etching-back or chemical mechanical polishing (CMP).

[c9] 15. The method of claim 7, wherein the conductive ma-

terial comprises copper or tungsten.

[c10] 16. The method of claim 7, wherein forming the word line and the capping layer comprises:
forming a conductive layer on the gate oxide layer;
forming a material layer on the conductive layer; and
patterning the material layer and the conductive layer perpendicular to the buried bit line to form the capping layer and the word line, respectively.

[c11] 17. The method of claim 7, wherein the word line comprises polysilicon.

[c12] 18. The method of claim 7, wherein the trench is defined after the self-aligned contact opening is defined in the steps of forming the trench and the self-aligned contact opening.